Experimental demonstration of a latch in clocked quantum-dot cellular automata

Alexei O. Orlov,[a] Ravi K. Kummamuru, Rajagopal Ramasubramaniam, Geza Toth, Craig S. Lent, Gary H. Bernstein, and Gregory L. Snider
Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana 46556

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We present an experimental demonstration of a latch in a clocked quantum-dot cellular automata (QCA) device. The device consists of three floating micron-size metal dots, connected in series by multiple tunnel junctions and controlled by capacitively coupled gates. The middle dot acts as an adjustable barrier to control single-electron tunneling between end dots. The position of a switching electron in the half cell is detected by a single-electron electrometer. We demonstrate ''latching'' of a single electron in the end dots controlled by the gate connected to the middle dot. This ability to lock an electron in a controllable way enables pipelining, power gain and reduced power dissipation in QCA arrays. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1355008]

Devices based on the quantum-dot cellular automata (QCA) computational paradigm[1] use single electrons in interacting quantum dots to encode and process binary information. Logic levels in QCA arrays of coupled quantum dots are represented by the spatial configurations of single electrons (referred to as ''polarizations'') rather than by voltage and current levels. The QCA approach offers significant potential advantages over transistor-based paradigms, especially with regards to their scalability to very high levels of complexity with ultralow power dissipation, since current switching is not required for QCA operation. In the last few years, significant progress has been made towards the experimental realization of QCA logic. Experiments[2] have demonstrated the basic premise of the QCA paradigm, i.e., the coding of information in the position of single electrons. It has been recently theoretically demonstrated that major improvements in QCA performance can be achieved by using clocked QCA design.[3] In a clocked cell, the tunnel barriers between quantum dots are modulated by the clock signal to control the time evolution of the charge state in the quantum dots. One of the most important advantages of clocked architecture is the ability to retain (''latch'') the charge after the input signal is removed. In this case, the locked electron provides a fixed input signal for the next cell. When used in a pipelined architecture, latches allow an array to be broken into subarrays, with each working on different parts of a computational problem. In contrast to the edge-driven cellular architecture where the input signal is the only source of energy, clocked cells can exhibit power gain[4] as well as resolve the issue of unidirectionality.[5] By switching the cells slowly compared to the characteristic tunneling time, quasi-adiabatic switching can be accomplished, leading to extremely low power dissipation.[3] Though current QCA implementations operate at sub 1 K temperatures, theoretical calculations[1,3] show that future metal nano-cluster and molecular implementations of QCA devices will work at liquid nitrogen and room temperatures.

Recently, a clocked QCA half cell proposed for the metal tunnel junction system,[6] was fabricated and tested.[7] In this device, an extra dot placed between the two dots of the half cell acts as a tunable barrier controlled by the clock signal [Fig. 1(a)]. When the clock signal is set to ''low,'' the half cell remains unpolarized (and the number of excess electrons on each island remains zero) even in the presence of a differential input signal. Raising the clock signal towards ''high'' results in an electron transfer from the middle dot to one of the end dots depending on the input.[8] Finally, when the clock is high, the electron is trapped on the dot to which it was transferred by the raising clock signal. In this case, the Coulomb barrier separating dots D1 and D3 is high, and the electron remains latched on an end dot when the input signal is set to zero or even reversed. For the reversed polarity of the input, this latched state becomes metastable. The escape of an electron from the latched state leads to a digital error. In our previous experiments with a three-dot device[7] we demonstrated the switching of a single electron by the clock signal, with the direction of an electron transfer defined by the input signal. However, the effect of latching was not observed in Ref. 7.

In this letter we report an experimental demonstration of a clocked QCA device acting as a latch. The device consists of three micron-size Al islands, ''dots,'' D1, D2 and D3

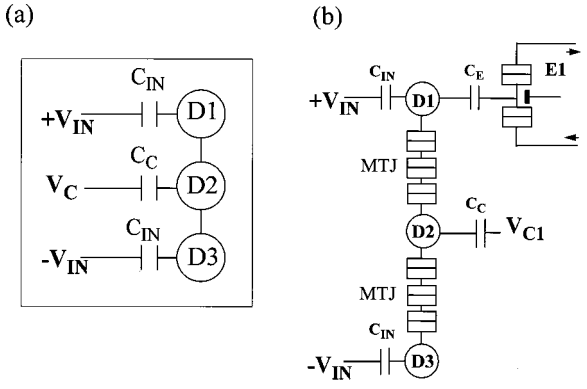

FIG. 1. (a) Schematic diagram of a clocked QCA half cell with three dots connected by tunnel barriers; (b) electrical diagram of the device and SET electrometer. Input differential signal is applied as shown.

[a]Electronic mail: orlov.1@nd.edu

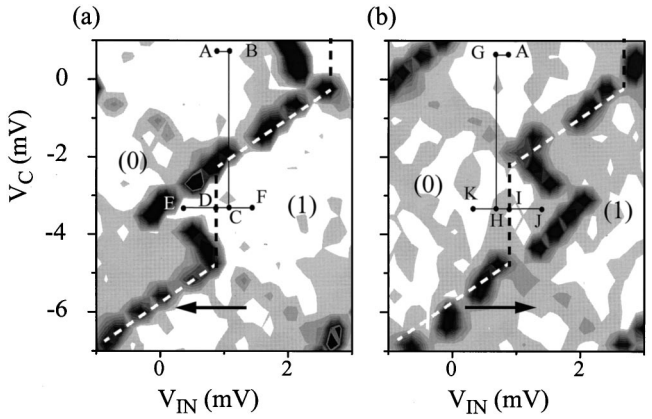

FIG. 2. ''Phase diagrams'' of stable charge configurations for two directions of the input voltage scans. To obtain the plot we scan input differential bias in the direction defined by the arrows. To highlight the borders between charge states, the acquired electrometer signal, I_E, is numerically differentiated and the absolute value of the derivative, abs(dI_E/dV_{IN}) is plotted as a gray scale map. The dashed line calculated using theory (see Ref. 6), marks the position of the equilibrium border between the ground state charge configurations on D1. Numbers in parentheses represent the number of excess electrons on D1.

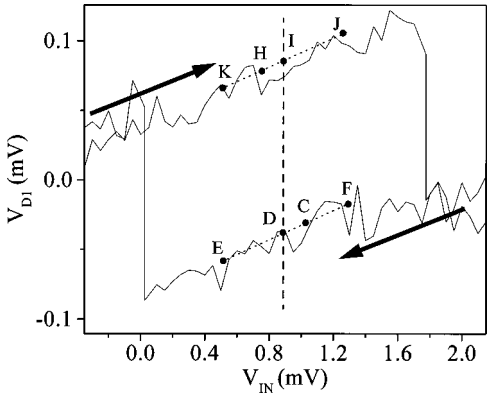

FIG. 3. Signal in the detector for two directions of the scan in the bistable region ($V_C = -3.2$ mV). The dashed vertical line delineates the position of an equilibrium border between charge configurations (see Fig. 2). Arrows depict the scan direction. Letters on the lines match those in Fig. 2, and dotted lines connecting the dots are a guide for the eye.

connected by two multiple tunnel junctions (MTJ) [Fig. 1(b)]. The signal ($+V_{IN}$, $-V_{IN}$) and clock (V_C) gates are capacitively coupled to the dots. Each MTJ consists of three tunnel junctions ($C_J \sim 300$ aF) and two small islands. To minimize parasitic coupling to these islands, the area of the islands in MTJs ($\sim 0.3 \times 0.08\ \mu m^2$) is made much smaller than the area of dots D1–D3 ($\sim 10 \times 0.08\ \mu m^2$). To measure a signal produced by a half cell, we use a single-electron electrometer E1 capacitively coupled to D1. The electron temperature of the device is 70 mK; the details of the experimental setup are described in Ref. 7.

To characterize the device, we first measure ''phase diagrams'' of stable charge configurations in the device in response to applied voltages V_{IN} and V_C (Fig. 2). The dark area on the diagram corresponds to the border between different charge states on D1. This allows us to find the appropriate magnitudes of the clock and input signals and set the working point (point A in Fig. 2). In contrast to the previous experiment,[7] a clear bistable behavior is observed. In agreement with theoretical models,[6,9] the location of the borders between charge states in the regions with bistability is defined by the direction of the input signal scan. The electrostatic potential on D1 (and D3) in these regions therefore shows hysteresis between the forward and reverse scans of the input bias (Fig. 3). The lower (upper) branch of the hysteresis loop corresponds to an electron trapped on D1 (D3).

Let us now consider the operation of a QCA latch. In the Toth–Lent clocking scheme,[6] all cells are first set to the null (unpolarized) mode with the clock signal set to low (in our experiment clock low corresponds to $V_C \approx 0.8$ mV, and clock high corresponds to $V_C \approx -3.2$ mV). After the input signal is applied, no electron transfer happens until the clock signal is set high. Here, the changing clock signal provides the necessary energy to transfer an electron from the middle dot to that dot for which positive input voltage is applied (active mode). Once the clock is set to high, the input signal can be removed, and the electron remains trapped on D1 or D3 until the clock is returned to low. This latched electron polarizes the cell. The resulting potential difference between top and bottom dot provides a signal to drive an adjacent half-cell which is activated by a separate clock line. Thus, a cycle describing the operation of a latch based on a QCA half cell is as follows: null–active–locked–active–null.[6]

Figure 4 represents the experimental demonstration of a QCA latch working in accordance with the described algorithm. To pre-set the device into the null state we used the phase-plot Fig. 2, where the working point A is set to $V_{g0} \approx 0.85$ mV and $V_{C0} \approx 0.8$ mV. (Offsets in the voltages V_{g0} and V_{C0} are caused by random background charge.) We will refer to Figs. 2 and 3 to explain the operation of the latch. Application of the input at t_0 corresponds to a movement from point A to point B in Fig. 2(a). As a result, at t_1, when the clock is set high [point C in Fig. 2(a)], an electron is transferred from D2 to D1. This situation corresponds to the lower branch of the hysteresis loop in Fig. 3 (point C). If an input signal of the opposite polarity is applied with the clock set low [at t_6, movement from A to G in Fig. 2(b)], then setting the clock high [at t_7, movement from G to H in Fig. 2(b)] leads to the opposite polarization of a half cell. In this case, an electron is transferred to D3 while the potential on

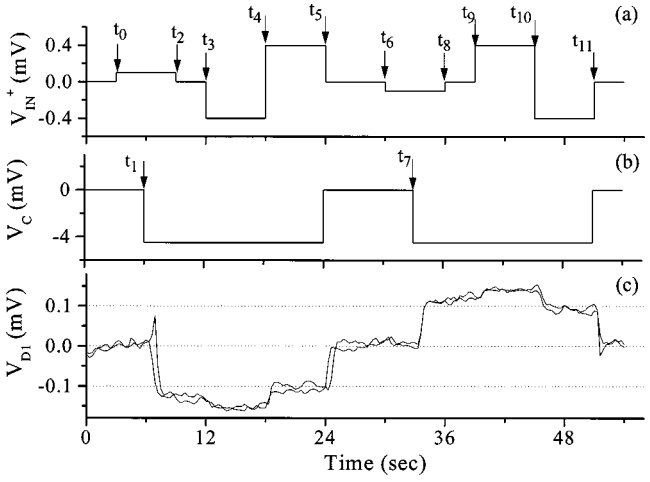

FIG. 4. Experimental demonstration of a functional QCA latch. The temporal response of half cell measured by the electrometer (c) is plotted for varying differential input (a) and clock (b) voltages. Two successive traces are shown.

D1 becomes more positive. This situation corresponds to the upper branch of the hysteresis loop in Fig. 3 (point H). As seen in Fig. 4, the device switches in the direction defined by the input, and its polarization remains constant when the input signal is removed [at t_2, movement from C to D in Figs. 2(a) and 3; and at t_8, movement from H to I in Figs. 2(b) and 3] until the clock signal is set to low (at t_5 and t_{11}). To demonstrate the ability of the latch to retain the stored electron for various settings of the input signal, an input voltage of both polarities is applied to the input gates after the clock is set high.[10] As one can see, the electron remains latched regardless of the input signal (movements from D to E at t_3, and then to F at t_4 in Figs. 2(a) and 3; and from I to J at t_9 and then to K at t_{10} in Figs. 2(b) and 3), provided the input signal remains within the bistability region in Fig. 2. A small change in the amplitude of the output voltage which is seen in Fig. 4 is the result of the sawtooth shape of the dot potential (Fig. 3). Thus, we experimentally demonstrate a latch acting in accordance with theoretical predictions.[6,9]

Let us discuss now possible sources of the digital errors in the latch. Dynamic errors[9] occur when the switching speed is too high compared to the tunneling rate ($\sim 10^{10}$ Hz for our junctions). Since our experiment is performed at very low frequencies (<0.1 Hz), the dynamic error can be neglected. Other possible sources of errors include (a) errors due to thermally activated processes; (b) errors caused by random background charge fluctuations; (c) errors caused by co-tunneling. To minimize the probability of the ''thermal'' error, $P_{\text{therm}} \propto \exp(-\Delta/kT)$,[9] where Δ is the energy difference between the end dots caused by the input signal ($\Delta \sim 0.2 E_C$[9] $\sim 50\,\mu$eV, where $E_C \sim 250\,\mu$eV is the charging energy of the dots), the experiment is performed at sufficiently low temperature ($kT \sim 6\,\mu$eV at 70 mK, $\Delta/kT \sim 8$). Our preliminary results show the disappearance of latching for temperatures higher than 300 mK ($\Delta/kT < 2$). Error caused by the fluctuations of the random background charge is a common problem for single-electron logic devices.[11] In our experiment a typical time during which the device remains unaffected by the fluctuation of the background charge is of the order of 500 s. Therefore, if the typical time of the experiment is 10–30 s, the probability of this type of error remains low. Finally, let us consider the error caused by the higher-order tunneling processes.[12] We calculate the escape rate, Γ, caused by co-tunneling,[12] for the junctions with the following parameters: junction resistance $R_J = 100\,\text{k}\Omega$; voltage across the junctions, $V = 250\,\mu$V; junction capacitance, $C_J = 0.3$ fF. This gives an estimate for a lifetime in the metastable state caused by co-tunneling, $\tau = 1/\Gamma$. In a cell with two junctions $\tau \sim 5$ ns, whereas for the system with six junctions connected in series, $\tau \sim 3000$ s. Therefore, to minimize the probability of this type of error for the experiment with the typical timeframe $\Delta t \sim 10$ s (and thus to satisfy the condition $\Delta t \ll \tau$), one needs to use MTJs to connect the dots. Thus, the use of MTJs minimizes the major source of error at the temperature of the experiment and makes it possible to demonstrate latching using a low-frequency setup. However, for high-speed applications, it will not be necessary to use MTJs.

In conclusion, we experimentally demonstrate a clocked bistable QCA device, capable of storing information in the position of a single electron. In this device, the direction of single-electron switching is defined by the input, while the switching itself, as well as the storage of the charge, is controlled by the clock. The realization of this device can be viewed as a first step towards functioning clocked QCA logic.

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